ABSTRACT

[Abstract of the Disclosure]

An integrated circuit having a memory cell array configuration capable of simultaneously performing data read and write operations is provided. The integrated circuit to which IOs are separately provided and to which a write address and a read address are simultaneously input during one period of a clock signal includes a plurality of memory blocks, each of the memory blocks having a plurality of sub-memory blocks, data memory blocks corresponding to the memory blocks, and a tag memory controlling unit, which writes data in the memory blocks or reads the data from the memory blocks in response to the write address or the read address. Even though the simultaneously-input write address and read address are the same, access to the same sub-memory block is not simultaneously performed. If each of the data memory block has the same size as the size of one sub-memory block, the data memory block may have the number of columns and rows different from the number of columns and rows of the sub-memory block. If the number of the sub-memory blocks is 2^N, each address of the tag memory controlling unit includes N+1 data bits, and N-bit of the N+1 data bits indicates a data memory address, and remaining 1-bit of the N+1 data bits indicates the valid determination information. In the integrated circuit (IC) having a memory cell configuration according to the present invention, a data read operation and a data write operation are simultaneously performed during one period of a clock signal, such that a period of the clock signal is reduced.

[Representative Drawing]

FIG. 2